LI-M114-FF
SPECIFICATION

Rev 1.1
Leopard Imaging Inc.

Contents

Version History

Version	Description	Release Date
1.0	First Release	9. Feb. 2015
1.1	Change the Lens (V1.4 module)	16. Mar. 2015

Key Information

Module Part#		LI-M114-FF
Module Size		90 mm (L) x 5.6 mm (W) x 3.9 mm(H)
Sensor Type		MT9M114
Array Size		1296 x 976
Supply Voltage	Digital	1.7 ~ 1.95V
	Analog	2.5 ~ 3.1V
	I/O	1.7 ~ 1.95 V or 2.5 ~ 3.1 V
	PLL	2.5 ~ 3.1 V
	PHY	1.7 ~ 1.95V
Optical format		1/6"
Focus(F.NO)		2.8
FOV (D)		60˚
Focal Length		2.54 mm
Focusing Range		30cm to infinity
TV Distortion		< 1 %
Pixel size		1.9 um x 1.9 um
Color filter array		RGB Bayer
Output format		YUV
Operating temperature		-30 ℃ to +70 ℃
Max. Frame Rate		30 fps full resolution, 36.7 fps 720p, 75 fps VGA , 120 fps QVGA2
Dynamic Range		70.8 dB
Max S/N ratio		37 dB
Responsivity		2.24 V/lux-sec(550 nm)
Shutter type		Electronic rolling shutter (ERS)
Power consumption		135 mW (for typical voltages and 720p output)
Input clock range		6 ~ 54MHz
Output pixel clock maximum		96 MHz

Pin Assignment

No.	Name	Pin type	Description
1	DGND	Ground	Digital ground
2	DOVDD1.8V/2.8V	Power	Power for I/O circuit
3	DGND	Ground	Digital ground
4	DGND	Ground	Digital ground
5	DOVDD1.8V/2.8V	Power	Power for I/O circuit
6	SDA	I/O	Two-wire serial interface data
7	DVDD1.8V	Power	Digital Power
8	SCL	Input	Two-wire serial interface clock
9	PWDN(NC)	NC	
10	DGND	Ground	Digital ground
11	RESET	Input/PU	Master reset signal, active LOW. This signal has an internal pull up
12	CLK-N	Output	Differential MIPI clock (sub-LVDS, negative)
13	DGND	Ground	Digital ground
14	CLK-P	Output	Differential MIPI clock (sub-LVDS, positive)
15	MCLK	Input	Master clock
16	DATA-N	Output	Differential MIPI data (sub-LVDS, negative)
17	DGND	Ground	Digital ground
18	DATA-P	Output	Differential MIPI data (sub-LVDS, positive)
19	AGND	Ground	Analog ground
20	DGND	Ground	Digital ground
21	AVDD2.8	Power	Analog power
22	DGND	Ground	Digital ground
23	AGND	Ground	Analog ground
24	DGND	Ground	Digital ground

Electrical Characteristics

1. Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit
		Min	Max	
V_{DD}_MAX	Core digital voltage	–0.3	2.4	V
V_{DD}_IO_MAX	I/O digital voltage	–0.3	4.0	V
V_{AA}_MAX	Analog voltage	–0.3	4.0	V
V_{DD}__PLL_MAX	PLL supply voltage	–0.3	4.0	V
V_{DD}_PHY_MAX	PHY supply voltage	–0.3	2.4	V
V_{IN}	DC input voltage	–0.3	VDD_IO + 0.3	V
I_{IN}	Transient input current (0.5 sec. duration)	–	150	mA
T_{OP}	Operating temperature (measure at junction)	–30	75	°C
T_{STG}[1]	Storage temperature	–40	85	°C

Notes: 1. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the product specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Core digital voltage	1.7	1.8	1.95	V
V_{DD}_IO	I/O digital voltage	2.5	2.8	3.1	V
		1.7	1.8	1.95	V
V_{AA}	Analog voltage	2.5	2.8	3.1	V
V_{DD}_PLL	PLL supply voltage	2.5	2.8	3.1	V
V_{DD}_PHY	PHY supply voltage	1.7	1.8	1.95	V
T_J	Operating temperature (at junction)	–30	55	70	°C

3. DC Characteristics

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{IH}	Input HIGH voltage		V_{DD}_IO * 0.7	–	V	1
V_{IL}	Input LOW voltage		–	V_{DD}_IO * 0.3	V	1
I_{IN}	Input leakage current	V_{IN} = 0V or V_{IN} = V_{DD}_IO		10	µA	2
V_{OH}	Output HIGH voltage	I_{OH} = 2 mA	V_{DD}_IO* 0.75		V	
V_{OL}	Output LOW voltage	I_{OH} = 2 mA	–	V_{DD}_IO * 0.25	V	

Notes: 1. V_{IL} and V_{IH} have min/max limitations specified by absolute ratings.
2. Excludes CONFIG and RESET_BAR as they have an internal pull-up resistor.

4. Operating Current Consumption

Default Setup Conditions: f_{EXTCLK} = 24 MHz, f_{PIXCLK} = 96 MHz, V_{AA} = V_{DD}_IO = V_{DD}_PLL = 2.8V, V_{DD} = V_{DD}_PHY = 1.8V, Tj = 70°C unless otherwise stated, PN9 enabled, specified under MIPI and Parallel output conditions

.

Symbol	Conditions	Min	Typ	Max	Unit
V_{DD}		1.7	1.8	1.95	V
V_{AA}		2.5	2.8	3.1	V
V_{DD}_PHY		1.7	1.8	1.95	V
V_{DD}_PLL		2.5	2.8	3.1	V
V_{DD}_IO	V_{DD}_IO = 2.8V	2.5	2.8	3.1	V
	V_{DD}_IO = 1.8V	1.7	1.8	1.95	V
I_{DD}	Full resolution 30 fps, parallel		39	50	mA
	720p, 30 fps, parallel		33	45	mA
	VGA binned, 60 fps, parallel		25	40	mA
	Full resolution, 30fps, MIPI		39	50	mA
	720p, 30 fps, MIPI		33	45	mA
	VGA binned, 60 fps, MIPI		25	40	mA
I_{AA}	Full resolution, 30 fps, parallel		19	35	mA
	720p, 30 fps, parallel		19	35	mA
	VGA binned, 60 fps, parallel		19	35	mA
	Full resolution, 30 fps, MIPI		19	35	mA
	720p, 30 fps, MIPI		19	35	mA
	VGA binned, 60 fps, MIPI		19	35	mA
I_{DD}_PLL	Full resolution, 30 fps, parallel		8	20	mA
	720p, 30 fps, parallel		8	20	mA
	VGA, 60 fps, parallel		8	20	mA
	Full resolution, 30f ps, MIPI		25	40	mA
	720p, 30 fps, MIPI		25	40	mA
	VGA binned, 60 fps, MIPI		25	40	mA
I_{DD}_PHY	Full resolution, 30 fps, parallel		0.02	0.5	mA
	720p, 30fps, parallel		0.02	0.5	mA
	VGA binned, 60 fps, parallel		0.02	0.5	mA
	Full resolution, 30 fps, MIPI		0.18	1	mA
	720p, 30 fps, MIPI		0.18	1	mA
	VGA binned, 60 fps, MIPI		0.18	1	mA
Total power consumption[1]	Full resolution, 30 fps, parallel		146		mW
	720p, 30fps, parallel		135		mW
	VGA binned, 60 fps, parallel		121		mW
	Full resolution, 30 fps, MIPI		194		mW
	720p, 30 fps, MIPI		183		mW
	VGA binned, 60 fps, MIPI		169		mW

Notes: 1. Total power excludes V_{DD}_IO current.

5. Standby Current Consumption (Parallel and MIPI)

Default Setup Conditions: f_{EXTCLK}=24 MHz, f_{PIXCLK}=96 MHz, V_{AA} = V_{DD}_IO = V_{DD}_PLL = 2.8V, V_{DD} = V_{DD}_PHY = 1.8V, T_J = 70°C unless otherwise stated

		Typical	Max	Unit
Soft Standby (CLK ON)	Total standby current in parallel and MIPI mode	1.4	3	mA
	Total power consumption in parallel and MIPI mode	2.5		mW
Soft Standby (CLK OFF)	Total standby current in parallel and MIPI mode	80	500	µA
	Total power consumption in parallel and MIPI mode	150		µW

Note: All power measurements exclude IO current.

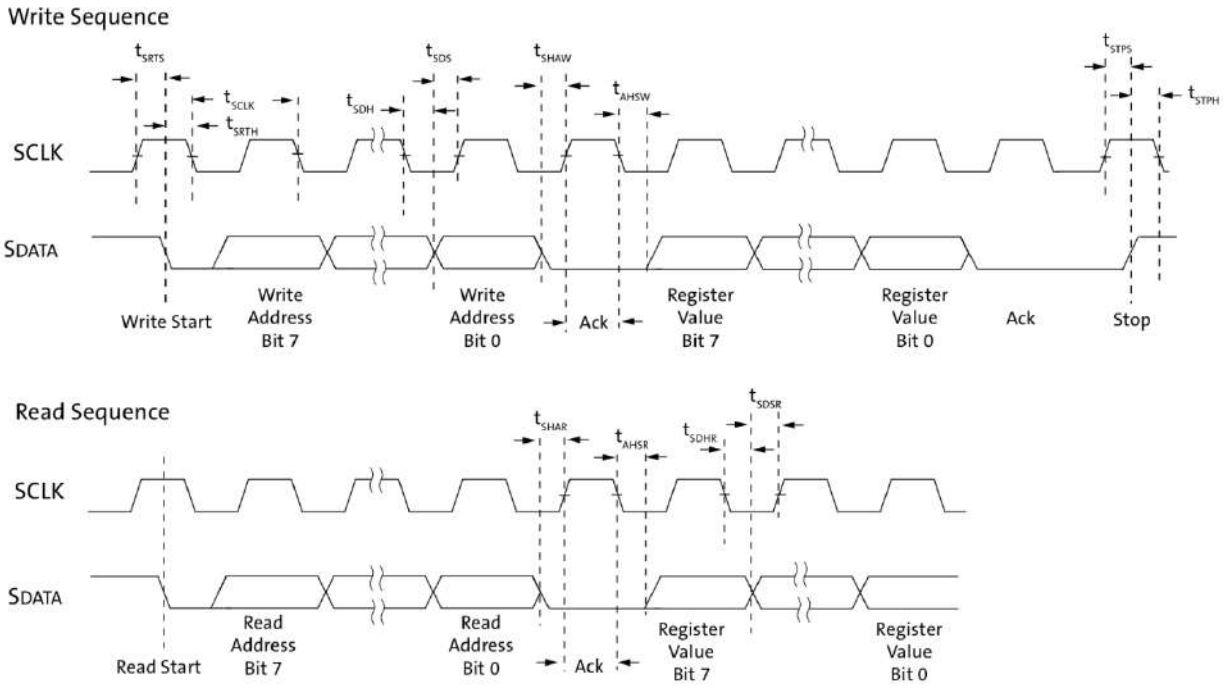
6. AC Electrical Characteristics

EXTCLK = 6–54 MHz; V_{DD} = V_{DD}_PHY = 1.8V; V_{DD}_IO = V_{AA} = V_{DD}_PLL = 2.8V; T_J = 25°C unless otherwise stated

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
f_{EXTCLK}	External clock frequency		6		54	MHz	1
D_{EXTCLK}	External input clock duty cycle		40	50	60	%	
t_{JITTER}	External input clock jitter		–	500	–	ps	2
t_{PD}	PIXCLK to data valid		–	2	5	ns	
t_{PFH}	PIXCLK to FV HIGH		–	2	5	ns	
t_{PLH}	PIXCLK to LV HIGH		–	2	5	ns	
t_{PFL}	PIXCLK to FV LOW		–	2	5	ns	
t_{PLL}	PIXCLK to LV LOW		–	2	5	ns	
t_{CP}	EXTCLK TO PIXCLK propagation delay	t_{PIXCLK} = PICXCLK period		0.1 x t_{PIXCLK}		ns	
PIXCLK slew rate							
	Slew = 4	V_{DD}_IO = 2.8V, PLL bypass, 6 MHz EXTCLK, C_{LOAD} = 35 pF	–	0.647	–	V/ns	
		V_{DD}_IO = 1.8V, PLL bypass, 6 MHz EXTCLK, C_{LOAD} = 35 pF	–	0.27	–	V/ns	
Output slew rate							
	Slew = 4	V_{DD}_IO = 2.8V, PLL bypass, 6 MHz EXTCLK, C_{LOAD} = 35 pF	–	0.229	–	V/ns	
		V_{DD}_IO = 1.8V, PLL bypass, 6 MHz EXTCLK, C_{LOAD} = 35 pF	–	0.112	–	V/ns	

Notes: 1. V_{IH}/V_{IL} restrictions apply.
2. Based on lab measurements. Could vary with noisier system-level electronics.

7. Two-Wire Serial Bus Timing Parameters

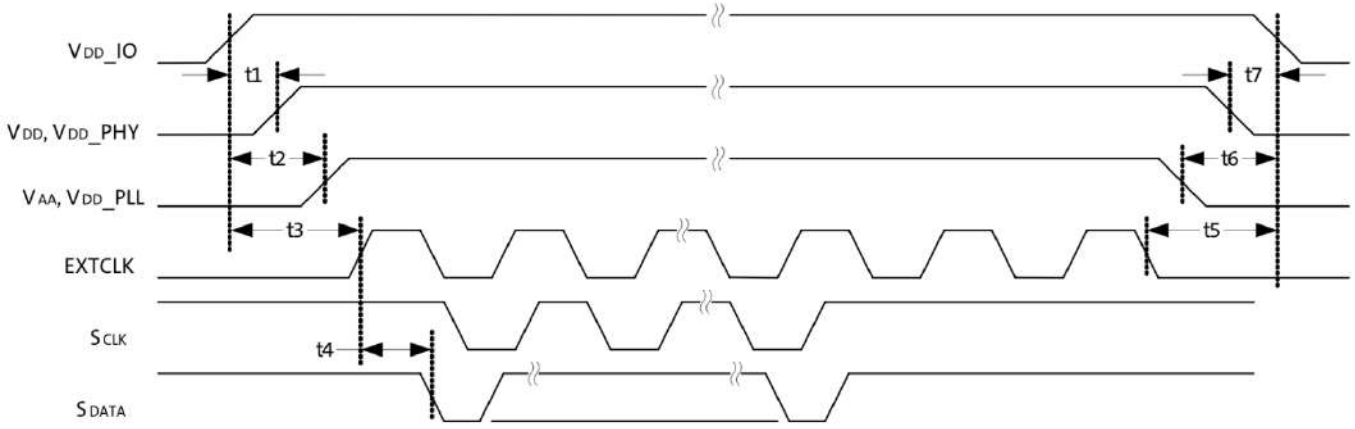


8. Two-Wire Serial Interface Timing Data

^{f}EXTCLK = 50 MHz; V_{DD} = 1.8V; V_{DD_IO} = 1.8V; V_{AA} = 2.8V; T_J = 70°C; C_{LOAD} = 68.5pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
^{f}SCLK	Serial interface input clock frequency		100	–	400	kHz
^{t}SCLK	Serial interface input clock period		10	–	2.5	µs
	SCLK duty cycle		45	50	55	%
^{t}r	SCLK/SDATA rise time		–	–	300	ns
^{t}SRTS	Start setup time	Master write to slave	600	–	–	
^{t}SRTH	Start hold time	Master write to slave	300	–	–	ns
^{t}SDH	SDATA hold	Master write to slave	300	–	650	ns
^{t}SDS	SDATA setup	Master write to slave	300	–	–	ns
^{t}SHAW	SDATA hold to ack	Master write to slave	150	–	–	ns
^{t}AHSW	Ack hold to SDATA	Master write to slave	150	–	–	ns
^{t}STPS	Stop setup time	Master write to slave	300	–	–	ns
^{t}STPH	Stop hold time	Master write to slave	600	–	–	ns
^{t}SHAR	SDATA hold to ack	Master read from slave	300	–	–	ns
^{t}AHSR	Ack hold to SDATA	Master read from slave	300	–	–	ns
^{t}SDHR	SDATA hold	Master read from slave	300	–	650	ns
^{t}SDSR	SDATA setup	Master read from slave	350	–	–	ns

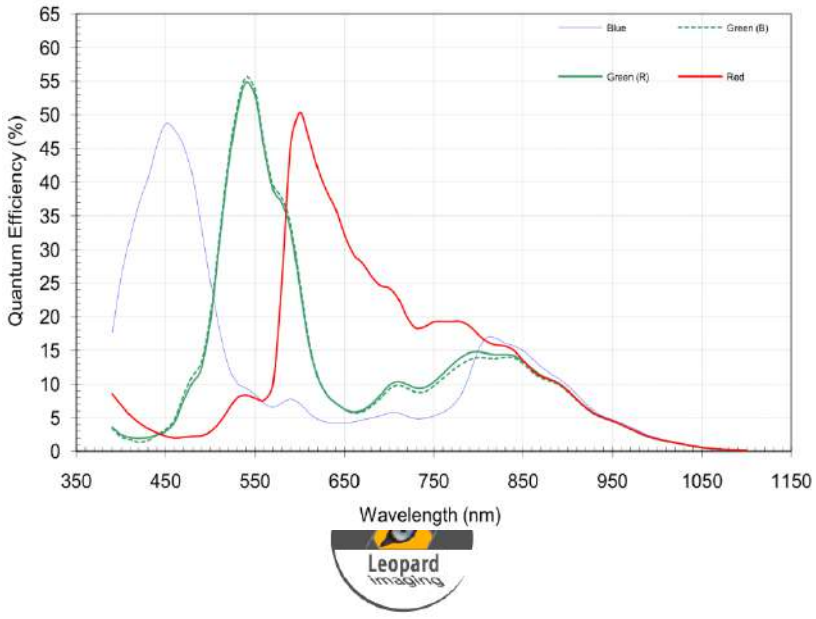
9. Power-Up and Power-Down Sequence

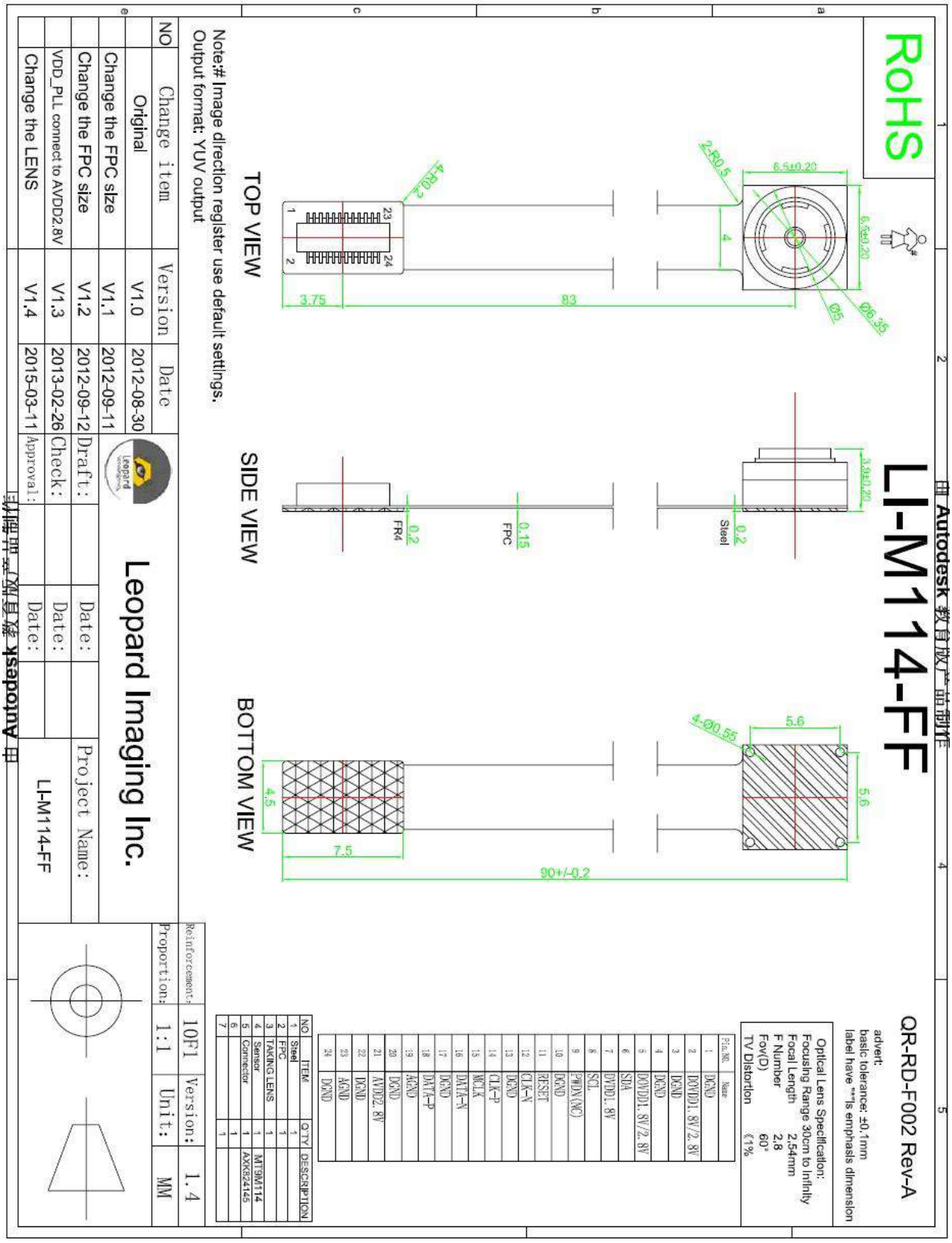


Symbol	Parameter	Min	Typ	Max	Unit
t1	Delay from VDD_IO to VDD and VDD_PHY	0	–	50	ms
t2	Delay from VDD_IO to VAA and VDD_PLL	0	–	50	ms
t3	EXTCLK activation	t2	–	–	ms
t4	First serial command[1, 2]	–	44.5	–	ms
t5	EXTCLK cutoff	t6	–	–	ms
t6	Delay from VAA and VDD_PLL to VDD_IO	0	–	50	ms
t7	Delay from VDD and VDD_PHY toVDD_IO	0	–	50	ms

Notes: 1. Under the condition of EXTCLK=24MHz and default settings with CONFIG=1.
2. The host should poll the Command register to determine when the device is initialized.

10. Typical Quantum Efficiency




RoHS
LI-M114-FF
QR-RD-F002 Rev-A
advert:
basic tolerance: ±0.1mm
label have "*"is emphasis dimension
Optical Lens Specification:
Focusing Range 30cm to Infinity
Focal Length 2.54mm
F Number 2.8
Fov(D) 60°
TV Distortion ≤1%
TOP VIEW
SIDE VIEW
BOTTOM VIEW
Note:# Image direction register use default settings.
Output format: YUV output
Leopard Imaging Inc.
LI-M114-FF
Reinforcement:
Proportion: 1:1
Unit: MM
Version: 1.4
10F1
Project Name:
Draft:
Check:
Approval:
Date:
Change item
Version
Date
Original V1.0 2012-08-30
Change the FPC size V1.1 2012-09-11
Change the FPC size V1.2 2012-09-12
VDD_PLL connect to AVDD2.8V V1.3 2013-02-26
Change the LENS V1.4 2015-03-11
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