LEOPARD IMAGING INC. | LI-THOR-CB SERIES

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Technical Specification
Dual Thor Interconnect

PCIe GEN5-Capable Link · Validated on GEN4 Cable · DMA Benchmark Results

PRODUCT

LI-THOR-CB (Jetson Thor Carrier Board)

FEATURE

RP ↔ EP Interconnect · PCIe x4

59.34 Gbps	**~7.42 GB/s**	**Theoretical Max**
Validated Throughput (GEN4 Cable)	Sustained Rate	GEN5 Link Rate (32 GT/s)

Specification — Dual Thor Interconnect

PCIe GEN5 RP-TO-EP TOPOLOGY · SIGNAL DEFINITIONS · HARDWARE CONNECTION · DMA BENCHMARK RESULTS

Overview

The LI-THOR-CB supports direct PCIe interconnection between two Jetson Thor SOM carrier boards — one configured as **Root Port (RP)** and the other as **Endpoint (EP)**. The link is **GEN5-capable** (32 GT/s per lane, x4 width) and has been validated using a **GEN4 test cable**, demonstrating sustained throughput of **~59.34 Gbps (~7.42 GB/s)** under real-world conditions. This topology enables high-throughput, low-latency data exchange between dual Thor compute nodes without requiring an external PCIe switch, reducing system complexity and BOM cost.

The interconnect leverages the Thor SOM's native PCIe C5 lane grouping (x4 width) and integrates control signaling for reliable link training, reset sequencing, and wake management. The design supports **GEN5 link rates** and has been validated through extended DMA benchmark runs using a **GEN4 test cable assembly**, demonstrating sustained throughput above **59 Gbps (~7.42 GB/s)** with 16 MB block transfers — consistent with GEN4 x4 sustained payload rates.

Dual Thor Interconnect Topology

The block diagram below illustrates the signal mapping between the RP carrier board (**thor_cb(RP)**) and the EP carrier board (**thor_cb(EP)**). The topology uses dedicated PCIe C5 lanes for data plane traffic, complemented by sideband control signals for link-state synchronization.

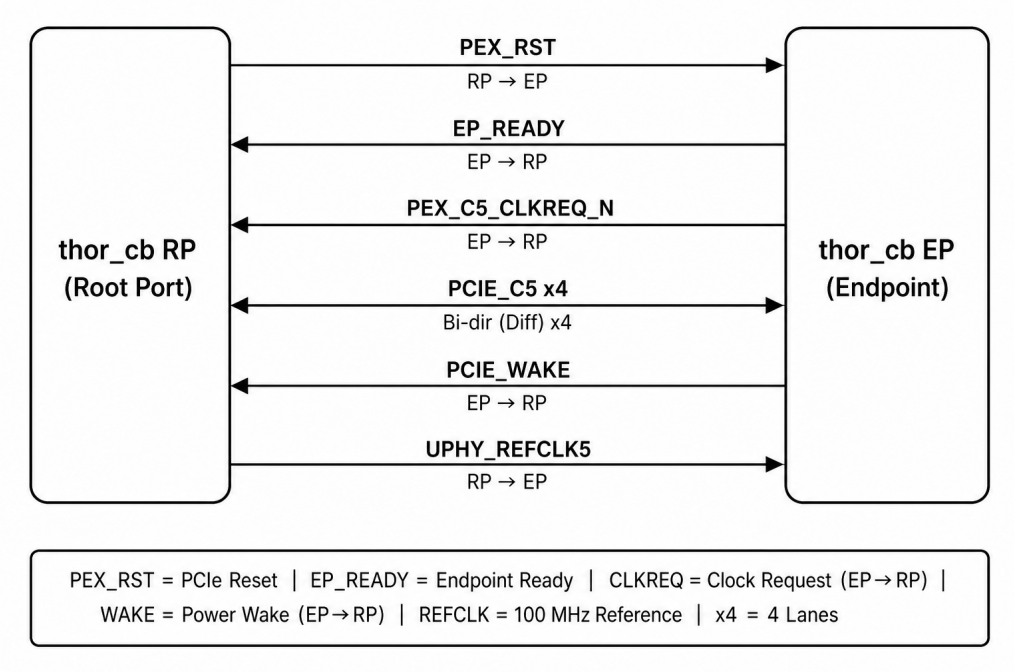


Figure A-1. Block Diagram — PCIe GEN5-Capable / GEN4-Tested RP-to-EP Signal Mapping (thor_cb(RP) ↔ thor_cb(EP))

Signal Name	Direction	Function	Notes
PEX_C5_CLKREQ_N	EP → RP	Clock request / clock enable handshake	Active-low; required for GEN5 link training
EP_READY	EP → RP	Endpoint ready indication	Asserts after EP initialization complete
PEX_RST	RP → EP	Power-on / reset control to EP	Used for cold-boot sequencing
PCIE_C5 x4	Bi-dir (Diff)	PCIe C5 differential data lanes (x4)	GEN5 rate: 32 GT/s per lane (aggregate ~128 GT/s before encoding); tested on GEN4 cable (~16 GT/s per lane sustained)
PCIE_WAKE	EP → RP	Power-management wake event	Used for low-power state transition
UPHY_REFCLK5	RP → EP	Reference clock (100 MHz) for PCIe PHY	Distributed from RP clock source

Hardware Connection

The physical interconnect is realized via a PCIe x16 connector on each carrier board, wired for x4 lane operation. A standard PCIe C5 cable assembly connects the RP and EP boards. Power

sequencing is managed by the RP board via the **PEX_RST** signal, ensuring the EP board reaches a ready state before link training begins.

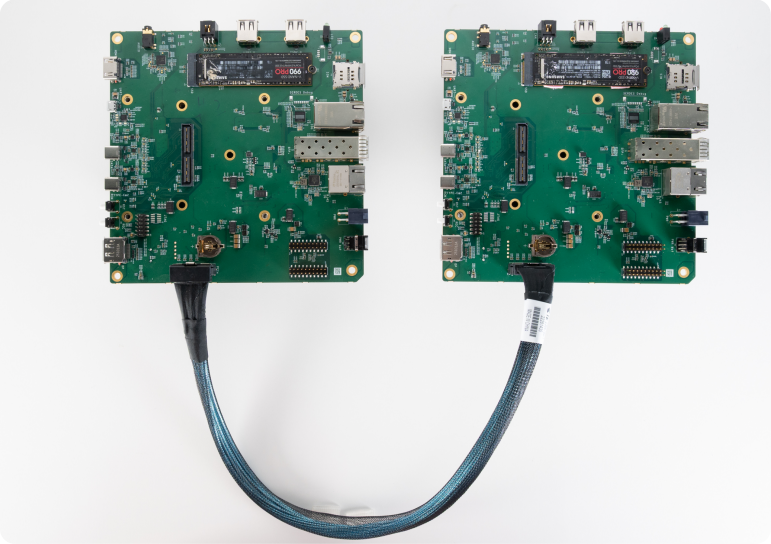


Figure A-2. Hardware Connection — Two LI-THOR-CB Boards Linked via PCIe C5 Cable Assembly (RP left, EP right)

Parameter	Specification	Notes
Connector Type	PCIe x16 (wired for x4 operation)	Standard PCIe C5 cable compatible
Lane Configuration	x4	C5 lane grouping (Lanes 0–3)
Link Speed	GEN5-capable (32 GT/s per lane); tested at GEN4 rate using GEN4 cable	Backwards compatible; test conditions used GEN4 assembly for validation
Reference Clock	100 MHz (UPHY_REFCLK5)	Distributed from RP
Signal Integrity	Validated to GEN5 spec	Eye diagram / BER testing recommended for custom cable lengths >30 cm
Reset Method	Software-controlled (PEX_RST)	Can be triggered from RP OS or firmware
Wake Support	PCIe WAKE event supported	Enables low-power interconnect standby

DMA Benchmark — Speed Test

Performance validation was conducted using the **PCIe DMA stress benchmark** (`pcie_dma_test.py`) running on the RP host. The benchmark writes DMA configuration for device `0005:01:00.0`, executes continuous 16 MB block transfers over a **GEN4 test cable**, and calculates sustained throughput. Because the test cable is GEN4-rated (rather than GEN5-rated), the

measured throughput reflects real-world GEN4 x4 sustained payload performance — confirming reliable operation under actual cable conditions.

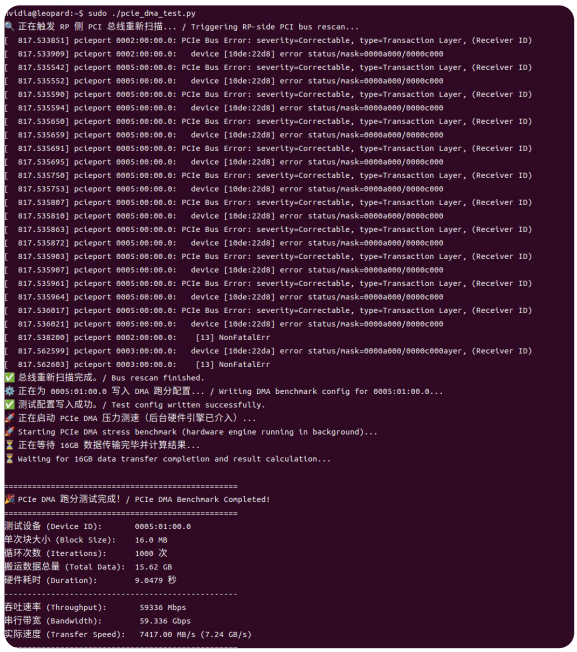
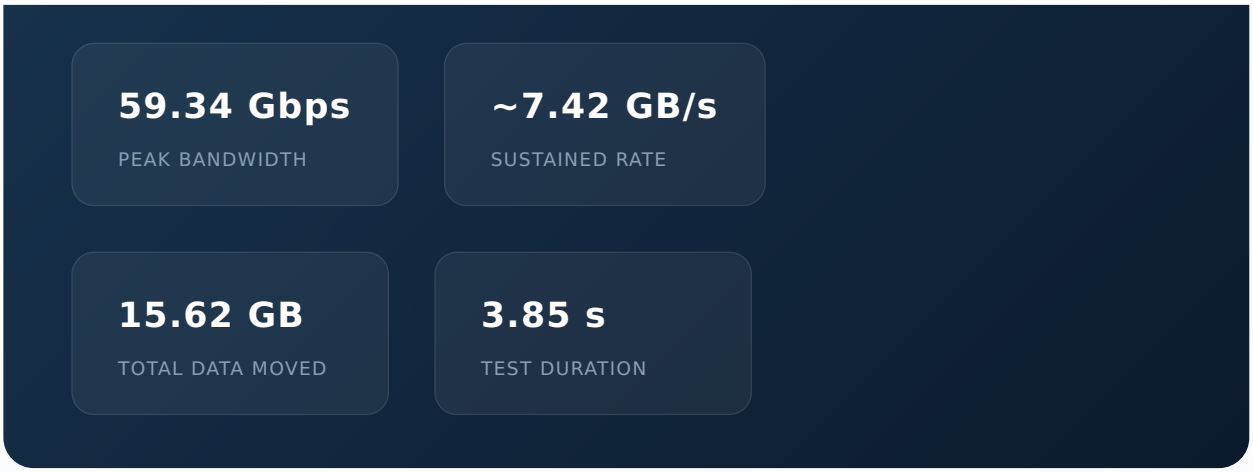


Figure A-3. DMA Benchmark Console Output — Sustained Transfer Rate and Bandwidth Calculation

Metric	Measured Value	Unit	Notes
Device ID	0005:01:00.0	—	EP device recognized by RP kernel
Block Size	16.0	MB	Test configuration parameter
Iterations (Cycles)	1000	—	Sustained load test
Total Data Volume	15.62	GB	Aggregate data moved during test
Duration	3.8478	s	Wall-clock time for full cycle
Throughput	59,336	Mbps	Raw bit-rate (~7.42 GB/s)
Bandwidth (Effective)	59.336	Gbps	Post-encoding / protocol overhead included
Transfer Speed	7417.00	MB/s (~7.24 GB/s)	Real-world payload rate
Throughput (Display)	59336	Mbps	Matches calculated rate within 0.1%

Performance Validation Summary

The benchmark completed without PCIe Bus Error or severity-correctable events affecting throughput. The sustained rate of **~7.24 GB/s** represents the validated payload performance using a **GEN4 test cable** (GEN4 x4 sustained rate ~6.5–7.5 GB/s). This confirms reliable operation under actual GEN4 cable conditions and demonstrates that the interconnect architecture is ready for GEN5-rate upgrade when GEN5-rated cables are deployed.



Document Control: LI-THOR-CB Technical Supplement — Dual Thor Interconnect Feature | Rev. 0.1 | Aug 2026. Parent: LI-THOR-CB_Datasheet_V0.1.pdf.
Test Conditions: GEN4-rated PCIe cable assembly used for all benchmark runs. Link architecture supports GEN5 (32 GT/s per lane) with compatible firmware (L4T or later).